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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,571	07/29/2003	Heon-Heung Leam	2522-025	8651

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MARGER JOHNSON & McCOLLOM, P.C.
1030 S.W. Morrison Street
Portland, OR 97205

EXAMINER

LE, THAO P

ART UNIT PAPER NUMBER

2818

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No. 10/630,571	Applicant(s) LEAM ET AL.	
	Examiner Thao P. Le	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 April 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 9-18 and 20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 9-18 and 20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. This office action is responsive to communication(s) filed on 04/05/05.

Claims 9-18, 20 are presented for examination.

Claims 9 and 20 have been amended.

Examiner took notice of remarks made on currently amended claims 9 and 20. Applicant's argument with respect to claims 9 and 20 on the ground that Sun (U.S. Patent No. 5,933,730) does not teach the newly added limitation of amended claims 9 and 20 reciting "etching the second gate spacers until a surface of the gate stack structures is exposed" has been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

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having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 9-16, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sun et al., U.S. Patent No. 5,933,730, and in view of Bae et al., U.S. Patent No. 6,693,013.

Regarding claims 9, 20, Sun et al. discloses a method of forming a non-volatile memory device comprising:

forming gate stack structures on a semiconductor substrate, the gate stack structures separated by a first space on a first area of the substrate and by a second space, wider than the first space, on a second area of the substrate adjacent to the first area (Figs. 9A-9C);

forming first spacers 714' on sidewalls of the gate stack structures, the first spacer material comprising an insulating material having relatively low dielectric constant (oxide spacer 714, Figs. 9D-9E).

forming second spacers on the first spacers to fill in the first space (oxide spacer 730, Figs. 9J-9K).

Sun discloses the first and second spacers are made of oxide which has relatively low dielectric constant but fails to disclose the second spacer material comprising an insulating material having a relatively high dielectric constant.

Bae et al. discloses a method of forming gate electrode comprising the first and second spacers whereas the first spacer 131 material comprising a relatively low

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dielectric constant (silicon oxide, dielectric constant of about 4.2), the second spacer 142 material comprising an insulating material having a relatively high dielectric constant (silicon nitride, dielectric constant of about 6.9) (Fig. 9; lines 35-52, Col. 4; lines 25-26, Col. 5).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form a second spacers made of relatively high dielectric constant material such as silicon nitride because the second spacers such as silicon nitride formed on the first spacers would prevent the first spacers and gate stack from silicide during salicidation process because oxygen finds it difficult to penetrate silicon nitride and because silicon nitride has low stress, good coverage, low pinhole densities.

Still regarding claims 9, 20, Sun fails to disclose the step of etching the second gate spacers until a surface of the gate stack structures is exposed.

Bae et al. discloses the step of etching the second gate spacer 142 to expose the surface of the gate stack structure (Figs. 8-9). It would have been obvious to one having ordinary skill in the art at the time the invention was made to expose the surface of the gate stack structure by etching the gate spacer because exposing the surface of the gate stack structures in order to form a silicide layer on the gate stack to reduce gate resistance or to form word lines or gate contacts on the gate stack.

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Regarding claim 10, both Sun et al. and Bae et al. disclose the first gate spacers comprises an oxide and Bae et al. discloses the second gate spacers comprise a nitride (lines 50-51, Col. 4).

Regarding claims 11-15, Sun and Bae do not disclose the thickness of the spacers or pressure used to form gate spacers, however, it would have been obvious to one having ordinary skill in the art that the thickness of the first and second spacers, the pressure used to form the spacers would have been optimum or working ranges to one having skill in the art. The selection of such parameters such as **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.**, would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.**, or in combination of the parameters would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art ... such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller* 105 USPQ233, 255 (CCPA 1955). See also *In re Waite* 77 USPQ 586 (CCPA 1948); *In re Scherl* 70 USPQ 204 (CCPA 1946); *In re Irmischer* 66 USPQ 314 (CCPA

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1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

Still regarding claim 15, Sun and Bae et al. disclose the method of claim 9 wherein forming the gate spacers comprising: depositing the first insulating layer, etching the first insulating layer to form the first spacer, depositing the second insulating layer, etching the second insulating layer to form the second spacer.

Regarding claim 16, Sun discloses the method as claimed in claim 9 wherein the gate stack structure is formed by sequentially stacking a tunnel dielectric layer, a floating gate, an integrated dielectric layer and a control gate (Figs. 9s).

4. Claims 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sun et al., U.S. Patent No. 5,933,730, and in view of Bae et al., U.S. Patent No. 6,693,013, and further in view of S. Wolf, "Silicon Processing for the VLSI era". Vol. 4, Lattice Press, Ca, pp. 603-615).

Regarding claims 17-18, Bae et al. discloses the step of forming silicide layer on the conductive gate, however, Bae et al. fails to disclose that the silicide layer comprises one selected from the group consisting of CoSi₂, TiSi₂, and NiSi₂. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form polysilicon-silicide in the structures of Sun and Bae et al. to obtain low resistivity and high thermal-stability. S. Wolf in "Silicon Processing for the VLSI era" also disclose the formation of polysilicon and silicide in the structures such as

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Sun's and Bae's to achieve small gate sheet-resistance. S.Wolf also suggests that CoSi_2 , TiSi_2 , and NiSi_2 are ideal candidates for self aligned silicide because they exhibit lower resistivities than silicides formed with the refractory metals such as W, Ta and they can reduce native oxide layers.

Conclusion

5. For the above reasons, it is believed that the rejections should be sustained.

Feature of an invention not found in the claims can be given no patentable weight in distinguishing the claimed invention over the prior art.

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP

' 706.07(a). Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

7. A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date

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of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1787. Other inquiries of this application should be called to (571) 272-1562 or the fax number (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thao P. Le
Examiner
AU 2818
April 17, 2005.